

FIG. 1A

170

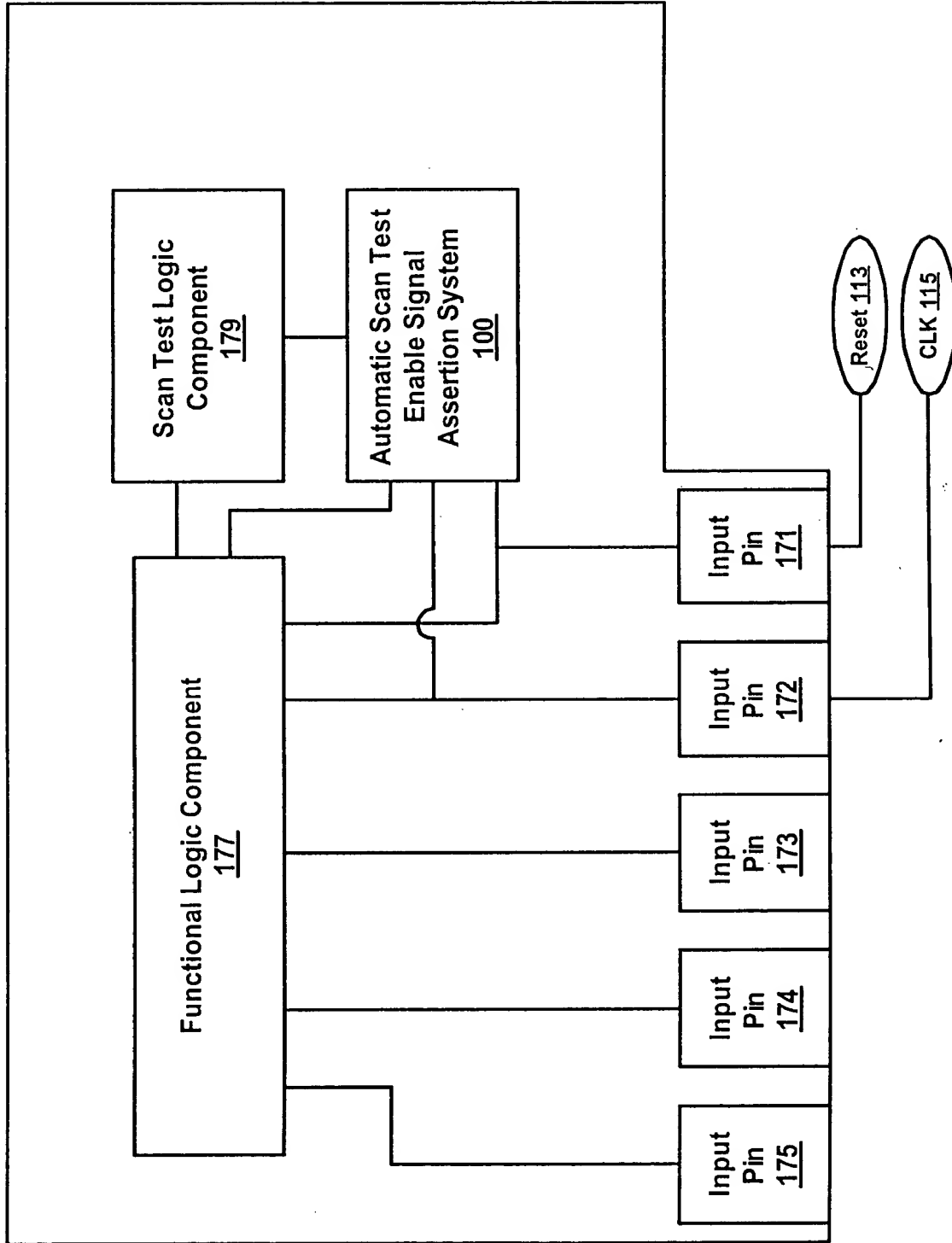


FIG. 1B



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200

```
/ *****
* *          BScanEnbN Module          * *
**-----**
***** /
/ /-----
module BScanEnbN (BScanEnbN,          // Output
                  pciClk, ioRstN ); //Input
/ /-----
output BScanEnbN ;
input  pciClk, ioRstN ;
reg    Q1_ioRstN, Q2_ioRstN, BScanEnbN ;
/ /-----Circuit -----
/ / Generating the BScanEnbN ;
always @ (posedge pciClk )
    begin
        Q1_ioRstN <- ioRstN;
    end
always @ (posedge pciClk)
    begin
        Q2_ioRstN <- Q1_ioRstN ;
    end
wire    D_BScanEnbN    --( Q1_ioRstN & Q2_ioRstN ) ;
always @ (posedge pciClk )
    begin
        BScanEnbN <- D_BScanEnbN;
    end
endmodule
```

FIG. 2

300

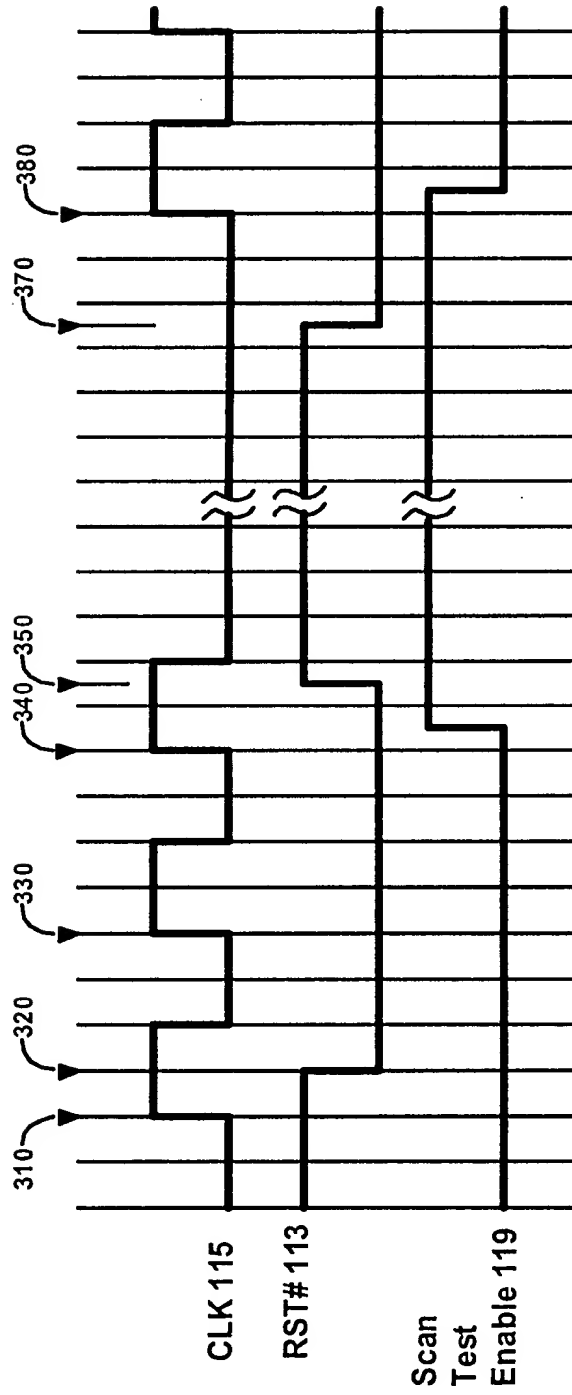


FIG. 3

400

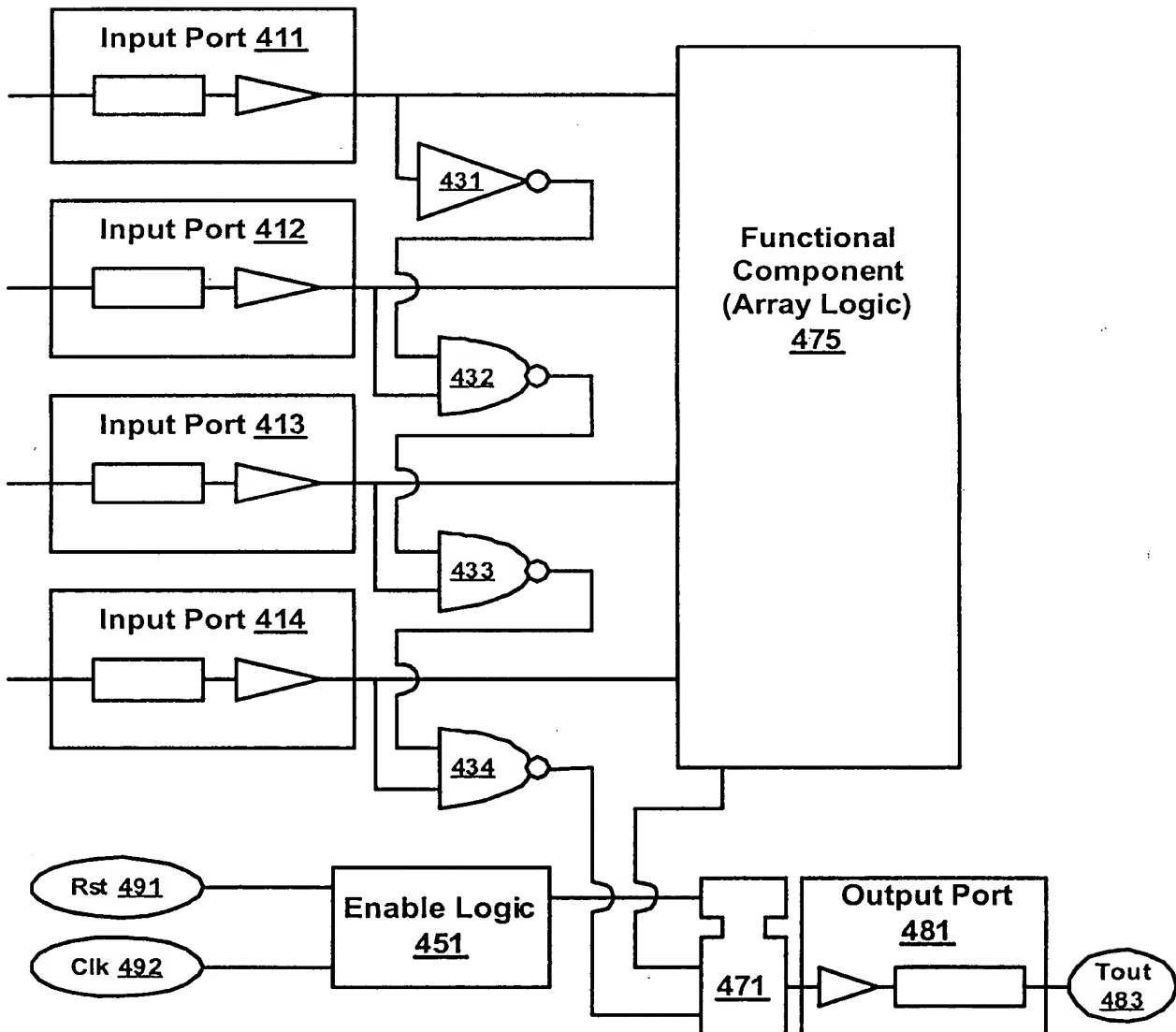
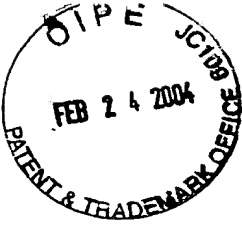


FIG. 4



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500

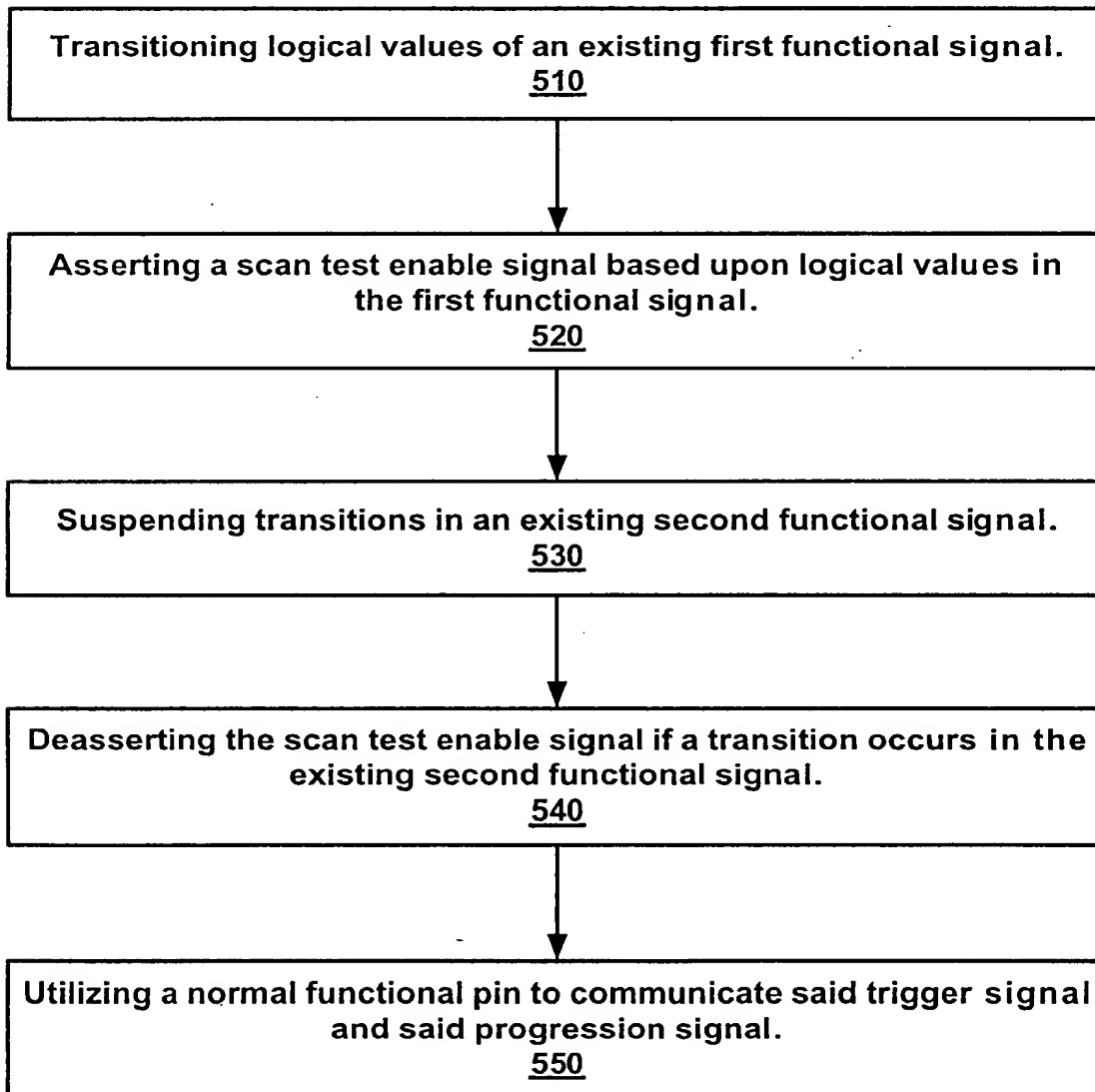


FIG. 5